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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/577,457	04/27/2006	Takamitsu Yamanaka	AI 409NP	5045

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EXAMINER	
LEE, JAE	

ART UNIT	PAPER NUMBER
2895	

MAIL DATE	DELIVERY MODE
09/28/2010	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/577,457	YAMANAKA, TAKAMITSU	
	Examiner	Art Unit	
	JAE LEE	2895	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 May 2010*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) *3 and 5-17* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4,18, and 19* is/are rejected.

7)☒ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1-4, 18, and 19 have been considered but are moot in view of the new ground(s) of rejection.

Election/Restrictions

Examiner is made aware of the restriction requirement mailed 10/03/2008 and response dated 10/28/2008 that an election without traverse has been made of claims 1, 2, and 4. Previous examiner inadvertently examined claim 3 which is in error. Consequently, claim 3 is hereby withdrawn from examination as per applicants' response to the restriction requirement dated 10/28/2009.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 2, 4, 18, and 19 are rejected under 35 U.S.C. 102(b) as being anticipated by Noda et al. (USP# 7,141,862 B2, hereinafter Noda et al.).

With regards to claim 1, Noda et al. teaches a semiconductor device comprising:

a semiconductor substrate (see Fig. 1, semiconductor substrate 10 present);

a first region defined on the semiconductor substrate and having a first device formation region isolated by a device isolation portion having an STI structure formed by filling an insulator in a trench formed in the semiconductor substrate, wherein a surface of the insulator of the STI structure and a surface of the semiconductor substrate are both arranged in a common plane (see Fig. 1, first region 10LVp / 10LVn, STi structure 22 with surface level with substrate 10);

a first device provided in the first device formation region (see Fig. 1, first device 200N);

a second region defined on the semiconductor substrate separately from the first region and having a second device formation region (see Fig. 1, second region 10HVn / 10HVp with second device formation region and separate from first region 10LVp / 10LVn); and

a second device provided in the second device formation region and having a higher breakdown voltage than the first device, the second device having a drift drain structure in which a LOCOS oxide film thicker than a gate insulation film thereof is disposed at an edge of a gate electrode thereof (see Fig. 1, second device 100N with drain drift structure 40 with LOCOS oxide 20a thicker than gate insulating film 60/ 62 and LOCOS oxide 20a disposed at an edge of gate 70); wherein

the device isolation portion includes, at a boundary between the first region and the second region, the STI structure in contact with the first region and the LOCOS oxide film in contact with the second region (see Fig. 1, boundary between 10LVn and

10HVn, STI structure 22 in contact with first region and LOCOS 20a in contact with second region), and

the insulator of the STI structure and the LOCOS oxide film are continuous at the boundary between the first region and the second region (see Fig. 1, STI and LOCOS are continuous at boundary).

With regards to claim 2, Noda et al. teaches a semiconductor device as set forth in claim 1, wherein the second device formation region is a region isolated by a device isolation portion formed by filling an insulator in a trench formed in the semiconductor substrate (see Fig. 1, col. 8, lines 10-30).

With regards to claim 4, Noda et al. teaches a semiconductor device as set forth in claim 1, wherein the first device has a smaller device size than the second device (see Fig. 1, first device in 100N smaller than second device 200N).

With regards to claim 18, Noda et al. teaches the semiconductor device according to claim 1, wherein the second region has a plurality of the second device formation regions isolated by a second device isolation portion including an STI portion formed by filling an insulator in a trench formed in the semiconductor substrate, and a LOCOS portion in contact with the second device (see Fig. 1, second region with a plurality of active regions with devices on top, STI structure 18 located between 200p

and 200n does isolate 100N and 100P from 200P, LOCOS 20b for example thermally contacts with second device 100N).

With regards to claim 19, Noda et al. teaches the semiconductor device according to claim 18, wherein the insulator of the STI portion is continuous with the LOCOS portion (see Fig. 1, STI structure 18 located between 200p and 200n is continuous with LOCOS 20b (i.e. no cessation or interruption, could be perceived as in no break when tracing a STI portion to LOCOS 20b along the lines / borders), if the trace runs into, for example, an outside boundary which is the result of separation into different entities, then continuous may not be present, “continuous” is a broad term).

Conclusion

4. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAE LEE whose telephone number is (571)270-1224. The examiner can normally be reached on Monday - Friday, 7:30 a.m. - 5:00 p.m. EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Drew Richards can be reached on 571-272-1736. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Jae Lee/
Examiner, Art Unit 2895

JML

/N. Drew Richards/
Supervisory Patent Examiner, Art Unit 2895